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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/032,513
Filing Date: October 26, 2001
Appellant(s): BEHRENS ET AL.

Paul D. Greeley
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/16/2007 appealing from the Office action mailed 09/28/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,324,664	FARWELL	11-2001
6,055,285	Alston	4-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farwell (US 6324664 B1) and further in view of Alston (US 6055285).

Regarding clam 1, Farwell discloses a testing unit for testing a device under test (DUT) comprising a signal generator that applies a stimulus signal to the DUT (figure 1 blocks 29 and 33 External test equipment and test bus controller column 4 lines 1-8) and a receiving unit that receives a response signal from the DUT on the applied stimulus signal (figure 1 blocks 29 and 33 External test equipment and test bus controller column 4 lines 1-8); and a synchronizing unit that synchronizes a data flow of the response signal between the DUT and the receiving unit, the synchronizing unit receives a first clock signal from the DUT and a second clock signal of the testing unit (figure 1 blocks 25 and 19, column 3 line 49 to column 4 line 23); the synchronizing unit includes a buffer for buffering data (figure 1 block 25, column 3 line 49 to column 4 line 23); a write unit for writing data from the DUT into the buffer (figure 1 block 19, column 3 line 49 to column 4 line 23); and a read unit for reading out data from the buffer to be provided to the receiving unit (figure 1 block 19, column 3 line 49 to column 4 line 23) .

Farwell doesn't specifically disclose the details that the first clock signal controls a write access onto the buffer; and that the second control signal controls a read access onto the buffer. Alston discloses a synchronizing unit for synchronizing a data flow of the response signal between two clock domains (figure 2 column 8 line 57 to column 9 line 12) where the first clock signal controls a write access onto the buffer (figure 2 blocks 140 column 8 lines 57-62); and that the second control signal controls a read access onto the buffer (figure 2 blocks 142 column 8 line 60 to column 9 line 3). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 2, Farwell and Alston disclose claim 1. Alston also discloses that the buffer comprises a register structure with a plurality of registers (figure 3 blocks 300, 304 and 306 column 9 line 49-50). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so

would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 3, Farwell and Alston disclose claim 2. Alston also discloses a write pointer that moves between the pluralities of registers for defining one of the plurality of registers to receive and buffer from one clock domain (figure 2 block 214 column 8 lines 62-66), and a read pointer that moves between the plurality of registers for defining one of the pluralities of registers to be read out (figure 2 block 216 column 9 lines 4-12). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 4, Farwell and Alston disclose claim 3. Alston also discloses that the write pointer is clocked by the first clock signal for successively writing successive data words from one clock domain to different registers (figure 3 block 122 and 106 column 9 lines 34-38), and the read pointer is clocked by the second clock

signal for successively reading out successive data words buffered in the plurality of registers (figure 5 block 132 and 108 column 17 lines 18-21). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 5, Farwell and Alston disclose claim 1. Alston also discloses that the write unit comprises a latch controlled by the first clock signal, so that successive data words can be latched with the first clock signal and thus successively written into the buffer (figure 3 block 300 column 9 lines 34-40). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 6, Farwell and Alston disclose claim 1. Alston also discloses that the buffer provides an initial delay time between a first valid write access and a first valid read access (figure 6 block 310 flip-flops 330-332-334-336 column 17 lines 23-28). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 7, Farwell and Alston disclose claim 6. Alston also discloses that the initial delay time is dependent on a maximum expected variation between such write and read accesses (figure 3 block 310 flip-flops 330-332-334-336 column 7 lines 23-28). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock

domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding clam 8, Farwell discloses a testing method for testing a device under test (DUT), the method comprising the steps of applying a stimulus signal to the DUT, where the DUT outputs data in response to the stimulus signal (figure 1 blocks 29 and 33 External test equipment and test bus controller column 4 lines 1-8); writing the data into a buffer, where a first clock signal is provided by the DUT (figure 1 blocks 19 and 25, column 3 line 49 to column 4 line 23); and reading the data from the buffer where a second clock provided by the receiving unit (figure 1 blocks 19 and 25, column 3 line 49 to column 4 line 23); and communicating the data from the buffer to the receiving unit (figure 1 blocks 19, 29 and 33, column 3 line 49 to column 4 line 23). Farwell doesn't specifically disclose that the writing employs the first clock signal that controls a write access to the buffer; and that the reading employs a second clock signal that controls a read access of the buffer. Alston discloses that the writing employs the first clock signal that controls a write access to the buffer (figure 2 blocks 140 column 8 lines 57-62); and that the reading employs a second clock signal that controls a read access of the buffer (figure 2 blocks 142 column 8 line 60 to column 9 line 3). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data

from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 9, Farwell and Alston disclose claim 8. Alston also discloses initializing a first valid write access or a first valid read access (figure 6 block 310 flip-flops 330-332-334-336 column 17 lines 23-28). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 10, Farwell and Alston disclose claim 8. Alston also discloses that the buffer provides an initial delay time between a first valid write access and a first valid read access (figure 6 block 310 flip-flops 330-332-334-336 column 17 lines 23-28). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the

transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

Regarding claim 11, Farwell and Alston disclose claim 10. Alston also discloses that the initial delay time is dependent on a maximum expected variation between such write and read accesses (figure 3 block 310 flip-flops 330-332-334-336 column 7 lines 23-28). Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

(10) Response to Argument

Regarding claim 1:

The Applicant contends, "However, whereas the Farwell et al. patent expressly states that the system accommodates asynchronous clocks, there is no apparent need to modify the Farwell et al. patent to include the synchronization circuit of the Alston patent. Moreover, if the Farwell et al. patent were modified to include the synchronization circuit of the Alston patent, such a modification would obviate the

manner in which modulo counter 27 and test bus controller 29 coordinate the writing of data to, and reading of data from, output memory 25, thus changing the principle of operation of the Farwell et al. patent. Hence, the cited combination of the Farwell et al. and Alston patent is **improper for purposes of a section 103(a) rejection** of claim 1. Accordingly, Appellants submit that claim 1 is patentable over the cited combination of the Farwell et al. and Alston patents" (emphasis in original).

The Examiner disagrees, and asserts, that, as indicated in the previous Office action, Farwell doesn't specifically disclose the details that the first clock signal controls a write access onto the buffer; and that the second control signal controls a read access onto the buffer, for this reason the Examiner uses a second reference that provides the details of how to transfer information between a first clock domain to a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous, Farwell (11-2001) patent doesn't provide these details. This doesn't change any principle of operation, Alston (4-2000) simply provide the details of one method of how to produce the transfer of these data between two different clock domains that are asynchronous.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re*

Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation used is from the secondary reference, as indicated in the previous Office action, that, Farwell and Alston are analogous art because they are from similar problem solving area of synchronization asynchronous clock domains. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to supplement the apparatus for testing disclosed by Farwell with the synchronization circuit disclosed by Alston. The suggestion/motivation for doing so would have been synchronizing the transfer of data from a transmitting circuit operating in a first clock domain to a receiving circuit operating in a second clock domain, where the first clock domain and the second clock domain are mutually asynchronous (Alston abstract and column 4 lines 14-24).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

For these reasons and the reasons indicated in the previous Office action the rejection of claim 1 is maintained.

Regarding claims 2-7:

The Applicant contends, "Claims 2 - 7 depend from claim 1. By virtue of this dependence, claims 2-7 are also patentable over the cited combination of the Farwell et al. and Alston patents".

The Examiner disagrees, and asserts, that, as indicated in the previous Office action, that because the rejection of claim 1 is maintained, the rejections of claims 2-7 are also maintained.

Regarding claim 8:

The Applicant contends, "Claim 8 includes a recital similar to that of claim 1, as presented above. Accordingly, claim 8, for reasoning similar to that provided in support of claim 1, is patentable over the cited combination of the Farwell et al. and Alston patents".

The Examiner disagrees, and asserts, that, as indicated in the previous Office action, that because the rejections of claim 1 is maintained, the rejection of claim 8 is also maintained.

Regarding claim 9-11:

The Applicant contends, "Claims 9 - 11 depend from claim 8. By virtue of this dependence, claims 9 - 11 are also patentable over the cited combination of the Farwell et al. and Alston patents".

The Examiner disagrees, and asserts, that, as indicated in the previous Office action, that because the rejections of claim 8 is maintained, the rejection of claims 9-1 are also maintained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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